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Hybrid Gate Dielectric Materials for Unconventional Electronic Circuitry

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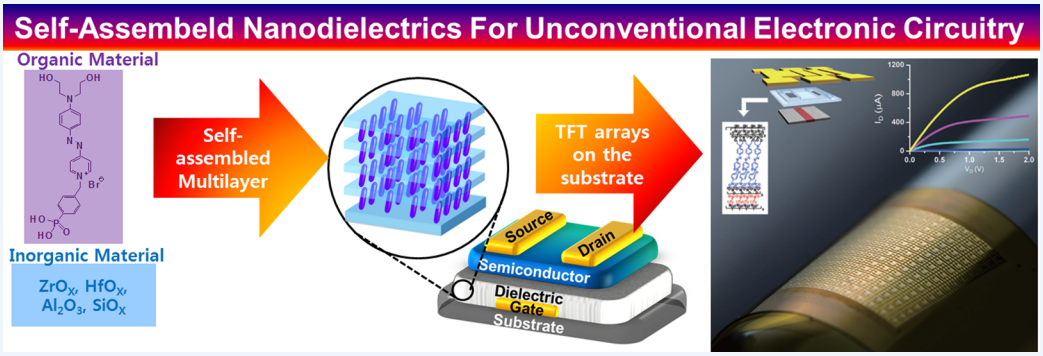

CONSPECTUS: Recent advances in semiconductor performance made possible by organic π-electron molecules, carbon-based nanomaterials, and metal oxides have been a central scientific and technological research focus over the past decade in the quest for flexible and transparent electronic products. However, advances in semiconductor materials require corresponding advances in compatible gate dielectric materials, which must exhibit excellent electrical properties such as large capacitance, high breakdown strength, low leakage current density, and mechanical flexibility on arbitrary substrates. Historically, conventional silicon dioxide (SiO_2) has dominated electronics as the preferred gate dielectric material in complementary metal oxide semiconductor (CMOS) integrated transistor circuitry. However, it does not satisfy many of the performance requirements for the aforementioned semiconductors due to its relatively low dielectric constant and intransigent processability. High-k inorganics such as hafnium dioxide (HfO_2) or zirconium dioxide (ZrO_2) offer some increases in performance, but scientists have great difficulty depositing these materials as smooth films at temperatures compatible with flexible plastic substrates. While various organic polymers are accessible via chemical synthesis and readily form films from solution, they typically exhibit low capacitances, and the corresponding transistors operate at unacceptably high voltages. More recently, researchers have combined the favorable properties of high-k metal oxides and π-electron organics to form processable, structurally well-defined, and robust self-assembled multilayer nanodielectrics, which enable high-performance transistors with a wide variety of unconventional semiconductors.

In this Account, we review recent advances in organic−inorganic hybrid gate dielectrics, fabricated by multilayer self-assembly, and their remarkable synergy with unconventional semiconductors. We first discuss the principals and functional importance of gate dielectric materials in thin-film transistor (TFT) operation. Next, we describe the design, fabrication, properties, and applications of solution-deposited multilayer organic−inorganic hybrid gate dielectrics, using self-assembly techniques, which provide bonding between the organic and inorganic layers. Finally, we discuss approaches for preparing analogous hybrid multilayers by vapor-phase growth and discuss the properties of these materials.

1. INTRODUCTION

Thin-film transistors (TFTs) fabricated from unconventional materials and by unconventional methodologies are of interest for future low-cost electronic applications, including RF-ID technologies, sensors, light-emitting diodes (LEDs), liquid crystal/OLED display backplane circuitry, and integrated optoelectronic devices.[1] The attractions of these systems include atomic-level tunability of properties,[2] solution processing via high-throughput roll-to-roll printing,[3] and low temperature (<150 °C) fabrication compatible with inexpensive, flexible plastic substrates.[4] This approach offers the possibility of inexpensive, large-area, flexible devices processed at far lower substrate temperatures and over far greater areas than conventional silicon-based technologies.[5]

Transistors are the key components used for current modulation and switching in all modern electronics. There are

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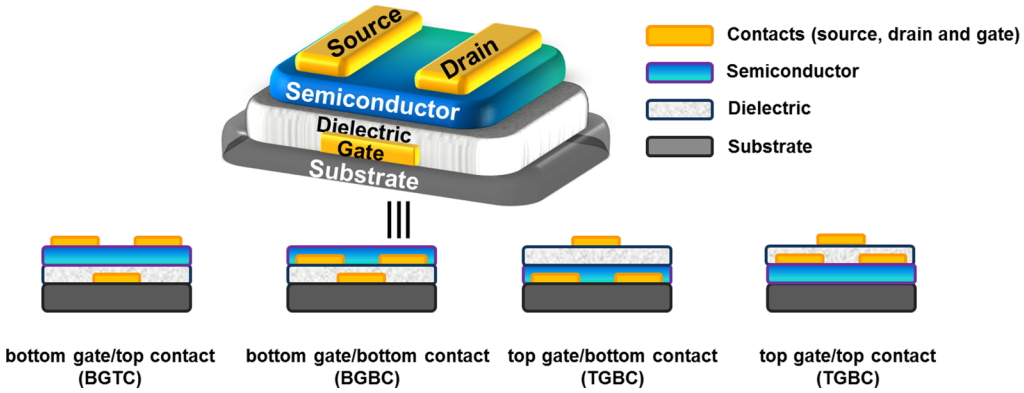

Figure 1. Typical thin-film transistor structures.

three fundamental TFT materials components: electrodes (source, drain, and gate), the semiconductor channel, and the gate dielectric. The arrangement of these components can be classified by the geometry of the gate (i.e., bottom-gate or top-gate) and contacts (i.e., bottom-contact or top-contact), leading to four common device geometries (Figure 1). The basic working principle of TFTs is that the current between source and drain contacts (I_{DS}) in saturation is modulated by the gate bias (V_G) according to eq 1 where W and L are the channel width and length, C_i is the dielectric capacitance per unit area, μ is the charge carrier mobility, V_G is the gate voltage, and V_T is the threshold voltage.

$$I_{DS} = \frac{W}{2L}\mu C_i(V_G - V_T)^2 \quad (1)$$

Over the past two decades, solution-processable organic, inorganic, and nanomaterial semiconductors have attracted much attention due to the aforementioned advantages over traditional silicon technologies.[6] Despite recent progress, a principal limitation of these semiconductors when integrated with conventional gate dielectric materials (SiO_2) is their low carrier mobilities, well below those of high-performance silicon-based materials.[7] These inferior transport characteristics, due primarily to SiO_2 defects such as charged oxide impurities, remote interface phonons, and interface traps, require additional source−drain (V_{DS}) to source−gate (V_G) bias (voltage) as compensation to achieve a target transistor current (I_{DS}), which in turn increases power consumption. For low power applications such as RF-ID tags, flat panel displays, and portable electronics, it is mandatory to achieve high TFT drain currents (I_{DS}) at the lowest operating voltages possible (ideally <4 V). According to eq 1, a feasible approach to achieve this is to increase the capacitance of the gate dielectric.

$$C_i = \varepsilon_0\frac{k}{d} \quad (2)$$

Note from eq 2 that increasing the dielectric constant (k) or decreasing the thickness (d) of the gate dielectric layer offers this additional capacitance. An increase in the k/d ratio is also necessary for efficient device size reduction (scaling), which supports low-power TFT operation. Importantly, from eq 1, enhancing the semiconductor mobility (μ), potentially enabled by a high-quality dielectric, can also increase the drain current for a given voltage, in addition to increases originating from capacitance.

High-k inorganic metal oxide (MO) dielectric films, such as HfO_2, Al_2O_3, or ZrO_2 have been grown by a variety of methods and exhibit well-defined dielectric properties.[8] However, high-quality MO dielectric films typically require high processing temperatures and/or capital-intensive vacuum deposition techniques to ensure acceptably low current leakage. Furthermore, most high-k MO films, particularly if crystalline, are generally too brittle for applications requiring flexible substrates. Thus, the demand for flexible plastic substrates and low-cost fabrication cannot easily be met with conventional high-k inorganic-only dielectrics. In contrast, many organic polymeric materials have processability advantages due to their mechanical flexibility, solubility, and capacity to form near-amorphous microstructures. Most importantly, they form films from solution and at low temperatures, enabling compatibility with solution-based coating/patterning techniques. However, typical polymer gate dielectrics have limits due to their relatively low dielectric constants and modest thermal stability.[9]

In contrast, organic−inorganic hybrids can, in optimum cases, synergistically combine the useful and distinctive properties of both classes of materials. Hybrid materials provide the optical, electrical, and environmental durability of inorganic materials, and the mechanical flexibility and properties tunability of π-electron organics. Combining these characteristics can thereby compensate for deficiencies in dielectric properties or processability, while often enhancing thermal and mechanical properties.[10] Notable examples of organic−inorganic hybrid gate dielectrics include using self-assembled monolayers (SAMs) with ultra-thin metal oxide films,[5,11] hybrid polymeric nanocomposite or bilayer materials,[12] and hybrid self-assembled multilayer structures.[14,15,28,29,31,32] Among these, self-assembled multilayers composed of well-defined organic precursor layers and inorganic metal oxide thin-films enable realization of new classes of robust functional materials with high degrees of order and structural control at the molecular level.

This Account focuses on the design, synthesis, properties tuning, and implementation of organic−inorganic multilayer gate dielectrics for TFTs fabricated with a variety of semiconductor classes. Recent applications and developments using hybrid materials in this area are summarized and analyzed. The discussion focuses on the two major approaches for preparing self-assembled multilayer hybrid dielectrics: solution and vapor phase deposition.

2. HYBRID MULTILAYER DIELECTRICS BY SOLUTION PHASE DEPOSITION

A key to utilizing layered organic−inorganic hybrid multilayers for electronics applications is the ability to prepare high-quality hybrid multilayers in the simplest, most reliable manner.

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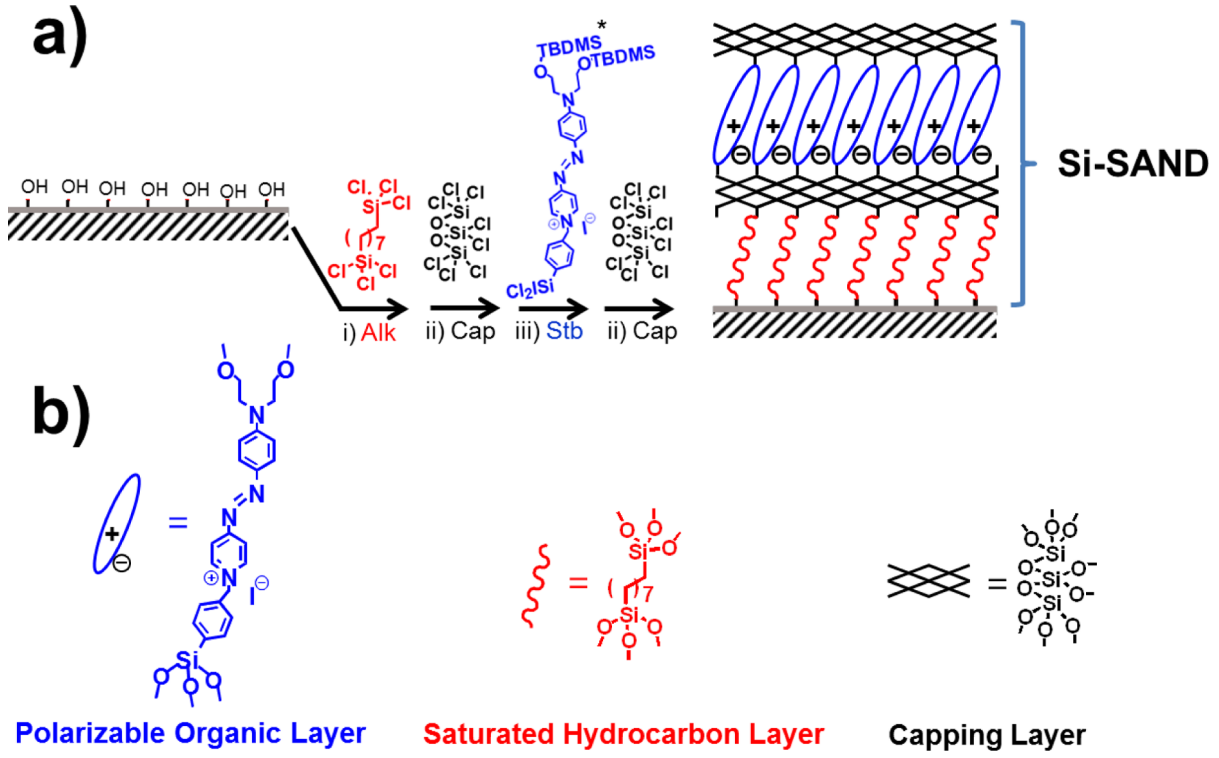

Figure 2. (a) Schematic representation of silane-based self-assembled nanodielectric (Si-SAND) multilayers, which can be sequentially deposited from solution. (b) Individual components of Si-SANDs. *TBDMS = *tert*-butyldimethylsilyl.

Layer-by-layer solution-based film growth using well-defined precursors enables the self-limiting assembly (self-assembly) of diverse, highly ordered functional materials. A variety of self-assembly approaches have been reported, often based on siloxane[13] or on metal−ligand coordination chemistry.[14]

2.1. Silane-Based Self-Assembled Nanodielectrics (Si-SAND)

First-generation hybrid gate dielectrics, referred to as silane-based self-assembled nanodielectrics (Si-SANDs), are grown by stepwise multilayer assembly using organosilane reagents (Figure 2).[15] The resulting hybrid materials contain 3D cross-linked thin-film networks grown from solution via self-limiting sequential deposition of chlorosilane building blocks, including saturated hydrocarbon layers, highly polarizable "push−pull" π-electron organic layers, and octachlorotrisiloxane-(Cl_3SiO-$(SiCl_2)OSiCl_3$)-derived capping layers. Capacitance−voltage ($C-V$) measurements on metal−insulator−semiconductor (MIS) structures reveal a range of capacitance (390−710 nF cm^{-2} at 10^2 Hz) depending on the combination of the organic and inorganic components. These Si-SANDs have several noteworthy characteristics that greatly enhance TFT performance: (1) large capacitance that reduces TFT operating voltage; (2) high thermal/chemical stability (e.g., 350 °C stability in air) compatible with a range of semiconductor processing conditions and operating environments; (3) marked tendency to suppress trapped charges at the dielectric−semiconductor interface.[14−24]

With Si-SAND gate dielectrics, impressive performance enhancements vs SiO_2 gate dielectrics are observed for ZnO, SnO_2, and In_2O_3 nanowire TFTs, with mobilities in the range 170−1500 $cm^2\ V^{-1}\ s^{-1}$ (typically ~10× greater than those with SiO_2).[16] Furthermore, arrays of Si-SAND/nanowire TFTs enable the fabrication of transparent active-matrix monochrome OLED displays.[17] Si-SAND was also investigated in TFTs with unpurified random network single-walled carbon nanotubes (SWCNTs) as the semiconductor,[18] achieving respectable mobilities (μ = 5.6 $cm^2\ V^{-1}\ s^{-1}$) and low threshold voltages (V_T = 0.2 V) with greatly reduced hysteresis and V_T shift versus devices with SiO_2 dielectrics. In the area of transparent oxide semiconductors (TOSs), Si-SAND compatibility was demonstrated by growing In_2O_3 thin films at 25 °C by ion-assisted deposition of both the semiconductor and source/drain layers (grown under different O_2 pressures) to enable high mobility, low voltage, and optically transparent ("invisible") TFTs:[19] μ = 120 $cm^2\ V^{-1}\ s^{-1}$, interfacial trap density $D = 10^{11}\ cm^{-2}$, V_T = 0.1, $I_{ON}/I_{OFF} = 10^5$, and subthreshold swing (SS) = 0.090 V $decade^{-1}$ with nearly hysteresis-free response. These metrics can be compared with SiO_2-gated devices where μ = 10 $cm^2\ V^{-1}\ s^{-1}$ and $I_{ON}/I_{OFF} = 10^5$. In subsequent studies, the same fabrication procedures using poly(ethyleneterephthalate) (PET) substrates afforded fully transparent and flexible In_2O_3 TFTs exhibiting μ = 20 $cm^2\ V^{-1}\ s^{-1}$ and $I_{ON}/I_{OFF} = 10^4$.[20] These results suggest new strategies for achieving "invisible" electronic circuitry as exemplified by polycrystalline In_2O_3 transistor arrays with hybrid dielectrics.

In related work, mechanically flexible, low operating voltage transistor logic gates (NOT, NAND, and NOR gates) were demonstrated using printed silicon nanomembranes with Si-SAND on thin plastic substrates (Kapton).[21] These transistors exhibit effective linear mobilities of ~680 $cm^2\ V^{-1}\ s^{-1}$, $I_{ON}/I_{OFF} > 10^7$, gate leakage current densities <2.8 × 10^{-7} A/cm^2, and SS ≈ 0.120 V $decade^{-1}$. Furthermore, Si-SAND/Si inverters show voltage gains as high as 4.8, and simple digital logic gates (NAND and NOR gates) demonstrate the possible application of these materials for flexible, high-performance digital integrated circuits.

In regard to device fabrication via solution processing, Si-SAND dielectrics were shown to be compatible with semiconducting CdSe films grown by chemical bath deposition

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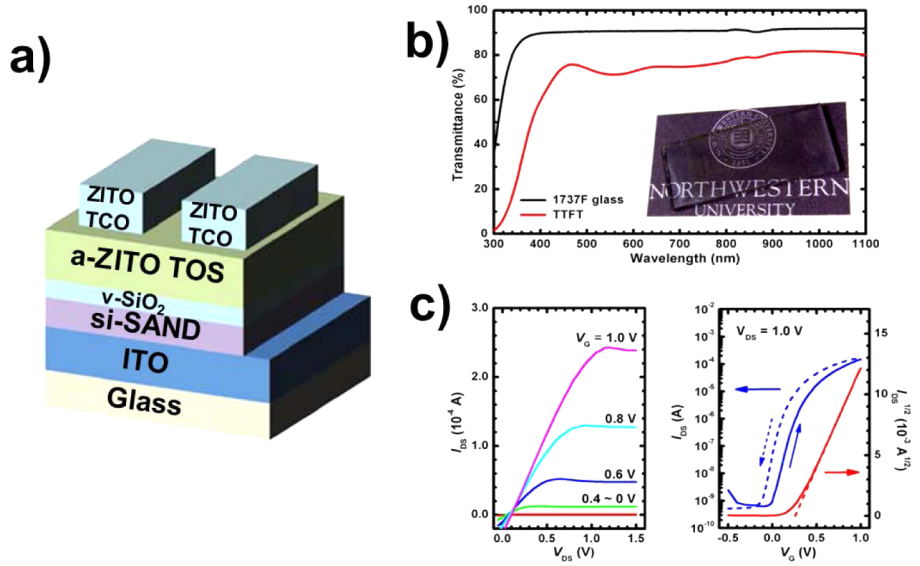

Figure 3. (a) Architecture of transparent a-ZITO (Zn−In−Sn−O) TFT fabricated on glass with the materials indicated. (b) Transmission optical spectrum of transparent array of TFTs (the inset shows a photograph of the TFT array on the glass). (c) Output plot showing good saturation characteristics with low operating voltages, and transfer plot showing minimal hysteresis. TOS = transparent oxide semiconductor; TOC = transparent oxide conductor; ITO = indium tin oxide. Adapted with permission from ref 26. Copyright 2011 Wiley-VCH Verlag GmbH & Co. KGaA.

(CBD) and annealed at 400−500 °C.[22] The mobilities of these films are ~57 $cm^2 V^{-1} s^{-1}$ with large I_{ON}/I_{OFF} (~10^5) and SS as low as 0.26 V $decade^{-1}$. In regard to solution-processed oxides, spin-coating In_2O_3 sol−gel precursor solutions on Si-SAND and annealing at 400 °C yields polycrystalline In_2O_3 films with TFT mobilities as high as ~44 $cm^2 V^{-1} s^{-1}$ with $I_{ON}/I_{OFF} > 10^7$ at <4 V operating bias.[23] Similarly, amorphous In−Sn−O films ([In]/[In + Sn] = 0.7) can be prepared by an analogous solution route and afford Si-SAND-based TFTs with $\mu \approx 10-20$ $cm^2 V^{-1} s^{-1}$ after annealing at relatively low temperature (250 °C).[24] In a subsequent paper, a detailed study of the Zn−In−Sn−O system yielded smooth, amorphous films with optimal transport properties after annealing at 400 °C. Here, a-Zn−In−Sn−O (a-ZITO) TFTs fabricated on Si-SAND exhibit $\mu \approx 90$ $cm^2 V^{-1} s^{-1}$, $I_{ON}/I_{OFF} \approx 10^5$, SS ≈ 0.2 V $decade^{-1}$, and operation at <2 V.[25]

Pulsed laser deposition (PLD) is a versatile film growth technique, and in related studies, it was shown that cross-linked, hexachlorodisiloxane ($Cl_3SiOSiCl_3$)-derived SiO_2 coatings greatly enhance Si-SAND resistance to PLD laser plume degradation while growing overlying oxide films on this dielectric, thereby expanding Si-SAND compatibility with a broad range of semiconductors.[26] For example, integrating Si-SAND and PLD-derived a-ZITO TOS films with a transparent conducting oxide (TCO) gate and source/drain electrodes yields optically transparent TFTs (Figure 3) with superlative performance parameters: $\mu \approx 140$ $cm^2 V^{-1} s^{-1}$, $I_{ON} > 10^{-4}$ A, $I_{ON}/I_{OFF} \approx 10^5$, SS ≈ 0.13 V $decade^{-1}$, and operating voltage ≈ 1.0 V.

Regarding the understanding of Si-SAND function, transport and computational studies indicate that the saturated hydrocarbon and SiO_x layers impart the insulating characteristics (transport via tunneling), while the π-electron layers provide the k (tunneling at low temperatures, hopping transport at higher temperatures).[27] Furthermore, quantitative analysis of Si-SAND dielectric breakdown via Weibull techniques shows that the breakdown statistics of these unconventional molecular dielectrics can be as uniform as those of conventional inorganic dielectrics.[28]

2.2. Zirconia-Based Self-Assembled Multilayer Nanodielectrics (Zr-SANDs)

In a second solution processed multilayer approach, zirconia-phosphonate self-assembled nanodielectrics (Zr-SANDs) incorporating highly polarizable phosphonic acid-based π-electron (PAE) layers interleaved with nanoscopic high-k zirconium oxide (ZrO_2) layers were synthesized and characterized (Figure 4).[29] The synthetic reagents are well-suited for self-assembly processes in ambient conditions, yielding well-structured multilayers, where ultra-thin ZrO_2 primer layers are spin-coated on hydroxyl-functionalized Si substrates, followed by baking and immersion in a phosphonic-acid (PA) functionalized precursor solution for self-assembly of the organic layer. Repeating this sequence results in structurally regular multilayers with tunable thicknesses (5−12 nm) characterized by X-ray reflectivity (XRR) and cross-sectional scanning transmission electron microscopy (STEM).

This flexible Zr-SAND synthetic approach offers high capacitance (465−750 nF/cm^2), low leakage current density (~10^{-7} A/cm^2 at 2 MV/cm), and thermal stability at 400 °C in ambient atmosphere. Zr-SAND dielectrics function effectively with both organic and inorganic semiconductors, exhibiting excellent TFT performance in terms of mobility (pentacene ~0.38 and Zn−Sn−O ~3.5 $cm^2 V^{-1} s^{-1}$) and I_{ON}/I_{OFF} (>10^6) at low operating bias (< ±4 V).[27] Moreover, these dielectrics can be modified by various PA-based hydrocarbon monolayers to further enhance TFT performance for n- or p-type organic semiconductors.[27] In related work, the compatibility of Zr-SAND with amorphous and polycrystalline In−Y−O (IYO) films grown via a low-temperature (200−300 °C) solution process utilizing "combustion" precursors was shown to afford low voltage (2 V) IYO TFTs with $\mu = 7.3$ $cm^2 V^{-1} s^{-1}$ ($T_{process}$ = 300 °C) and 5.0 $cm^2 V^{-1} s^{-1}$ ($T_{process}$ = 250 °C), and $I_{ON}/I_{OFF} > 10^5$.[30] This integration of combustion-derived amorphous oxide films with hybrid nanodielectrics points to future opportunities in novel materials implementation at temperatures compatible with flexible plastic substrates.

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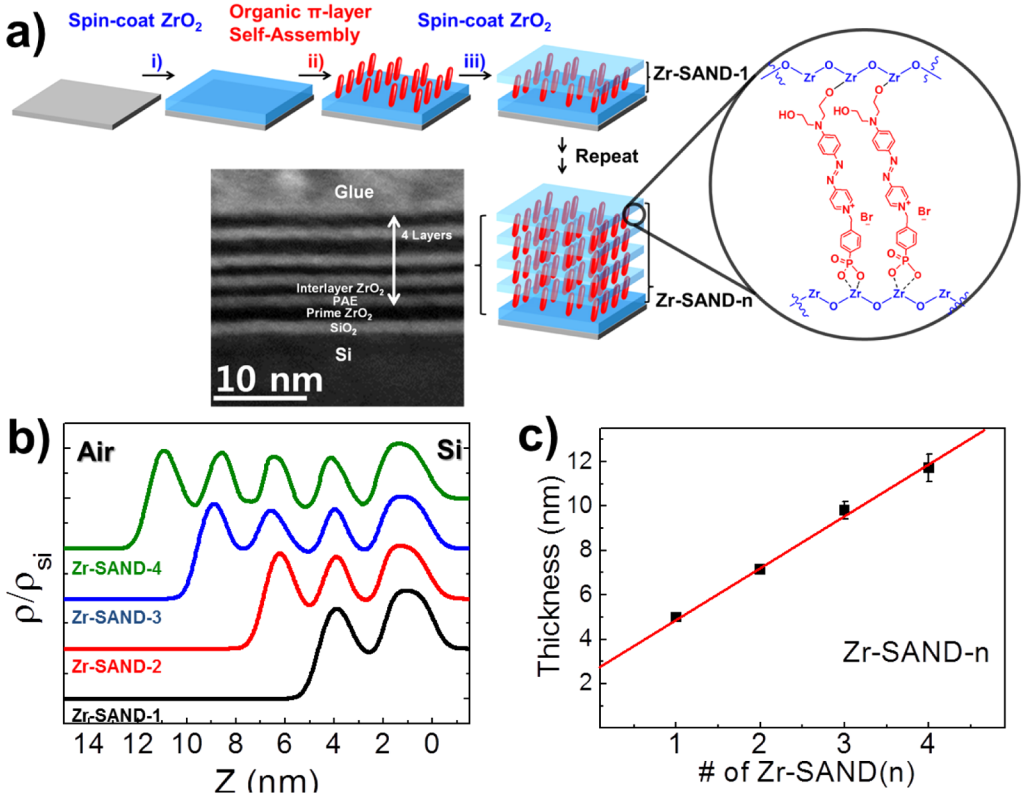

Figure 4. (a) Fabrication procedure for Zr-phosphonate self-assembled nanodielectric (Zr-SAND): (i) spin-coat ZrO_2 for prime layer; (ii) self-assembly of phosphonic acid-based organic π-electron layer; (i) spin-coat ZrO_2 for interlayer (inset shows cross-sectional TEM image of the Zr-SAND film interface; labels indicate the layer identities). (b) Specular X-ray reflectivity (XRR)-derived electron density profiles (normalized to ρ_{si}) as a function of height z above the Si substrate. (c) XRR-derived film thickness (nm) data as a function of the number of Zr-SAND prepared via the procedure of panel a. Adapted with permission from ref 29. Copyright 2011 American Chemical Society.

The uniformity of the dielectric breakdown voltage distribution for several thicknesses of Zr-SANDs was characterized using Weibull statistical analysis.[31] Two regimes of breakdown behavior are observed: thicker multilayers (>5 nm) are well described by the Weibull distribution, while thinner multilayers (≤5 nm thick) exhibit bends in the Weibull plot of breakdown voltage, suggesting multiple characteristic mechanisms. Interestingly, both the degree of uniformity and the effective dielectric breakdown field are observed to be greater for thinner layers than for thicker layers of Zr-SAND, implying that the thinner layer structure is more promising for device applications.

2.3. Hafinia-Based Self-Assembled Nanodielectrics (Hf-SANDs)

Hafnium oxide (HfO_x)-based SAND materials (Hf-SAND) were recently investigated in an effort to increase the k-enhancing PAE π-organic layer surface coverage via the greater HfO_x affinity for acids versus that of ZrO_x, and to expand the library of compatible oxide semiconductors (Figure 5a).[32] An earlier TFT study of Si-SAND with SWCNTs[16] motivated their use to probe the dielectric characteristics of Hf-SAND. Advances in SWCNT purification[33] along with the very large capacitance of 1.1 μF/cm^2 for single-layer Hf-SAND determined in this work (~10× greater than that in the original Si-SAND), enabled high-performance semiconductor-enriched SWCNT TFTs (Figure 5b). Outstanding device performance was obtained with $I_{DS} \approx 10$ mA using only $V_{DS} \approx 1$ V and $V_G \approx 3$ V, offering record transconductance (g_m) of 5.5 mS and record-matching SS of ~0.15 V decade^{-1},[34] indicative of low interface trap density. Gate leakage current was limited to ~2 nA at +2 V V_G even with large I_{DS} in the TFT channel. The highly uniform and conformal coating possible with HfO_x and the organic nanolayers provides smooth interfaces of ~2 Å rms roughness with limited pinhole defects, such that large-area TFT devices (850 μm × 250 μm) can reliably be produced on a 4.7 nm thick Hf-SAND layer (Figure 5b). Near record intrinsic mobilities (μ_{IN}) of ~140 cm^2 V^{-1} s^{-1} demonstrate the ability of Hf-SAND to efficiently drive dense SWCNT networks (15 SWCNTs/μm), historically difficult for globally back-gated SWCNT TFT geometries.[35] The excellent capacitive coupling of the semiconductor and gate offers simultaneously large I_{ON}/I_{OFF} (~10^6), I_{DS}, μ, and unprecedented g_m.[36,37]

Finally, the low temperature (<150 °C) solution-based growth of Hf-SAND opens the possibility of using inkjet-printable semiconducting In−Ga−Zn−O (IGZO) for TFT fabrication.[38] Thus, a new low-temperature "combustion" chemistry route to IGZO thin films was developed that produces high-mobility films at $T_{process}$ = 300 °C. Using SiO_2 and in-house grown atomic layer deposition (ALD) HfO_2 as control dielectrics, Hf-SAND-gated, inkjet-printed IGZO TFTs (Figure 5c) demonstrate a record electron mobility $\mu = 20.6 \pm 4.3$ cm^2 V^{-1} s^{-1}, steep SS ≈ 0.15 V decade^{-1}, near zero V_T, and the ability to achieve $I_{DS} \approx 1$ mA with <2 V V_{DS} and <2 V V_G. This μ is nearly 4× greater than the control devices (~5 cm^2 V^{-1} s^{-1}), where the origin of the mobility enhancement is attributed to low levels of dielectric fixed charge, reducing Coulombic scattering of carriers in the IGZO semiconductor layer.[39] Thus, Hf-SAND not only offers the large capacitance possible with other ALD-grown high-k oxide materials, but limits the impact of oxide fixed charge,

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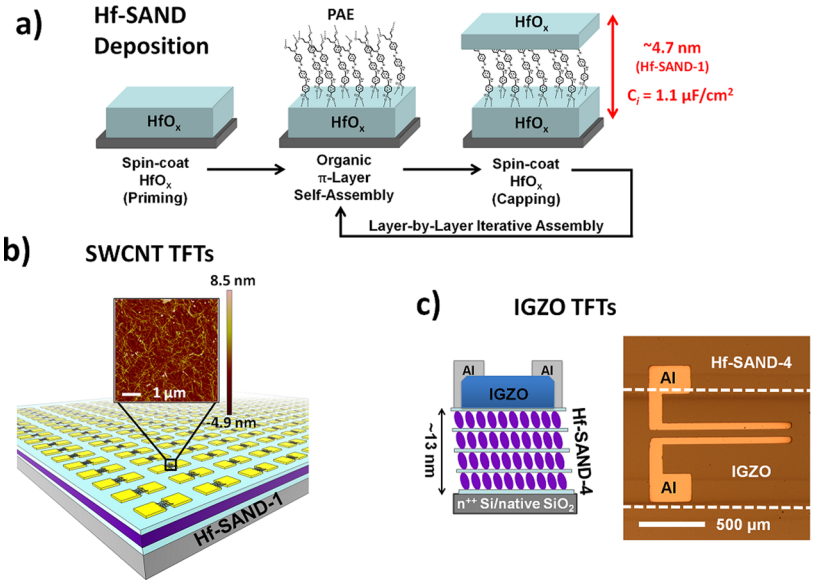

Figure 5. (a) Solution-phase Hf-SAND self-assembly procedure. (b) Schematic SWCNT/Hf-SAND TFT arrays, with inset atomic force micrograph showing a random network of SWCNTs in the TFT channel. (c) IGZO TFTs produced by inkjet printing (right) utilizing the multilayer variant of Hf-SAND schematically shown on the left. Panels a and b adapted with permission from ref 32 and panel c from ref 39. Copyright 2013 American Chemical Society.

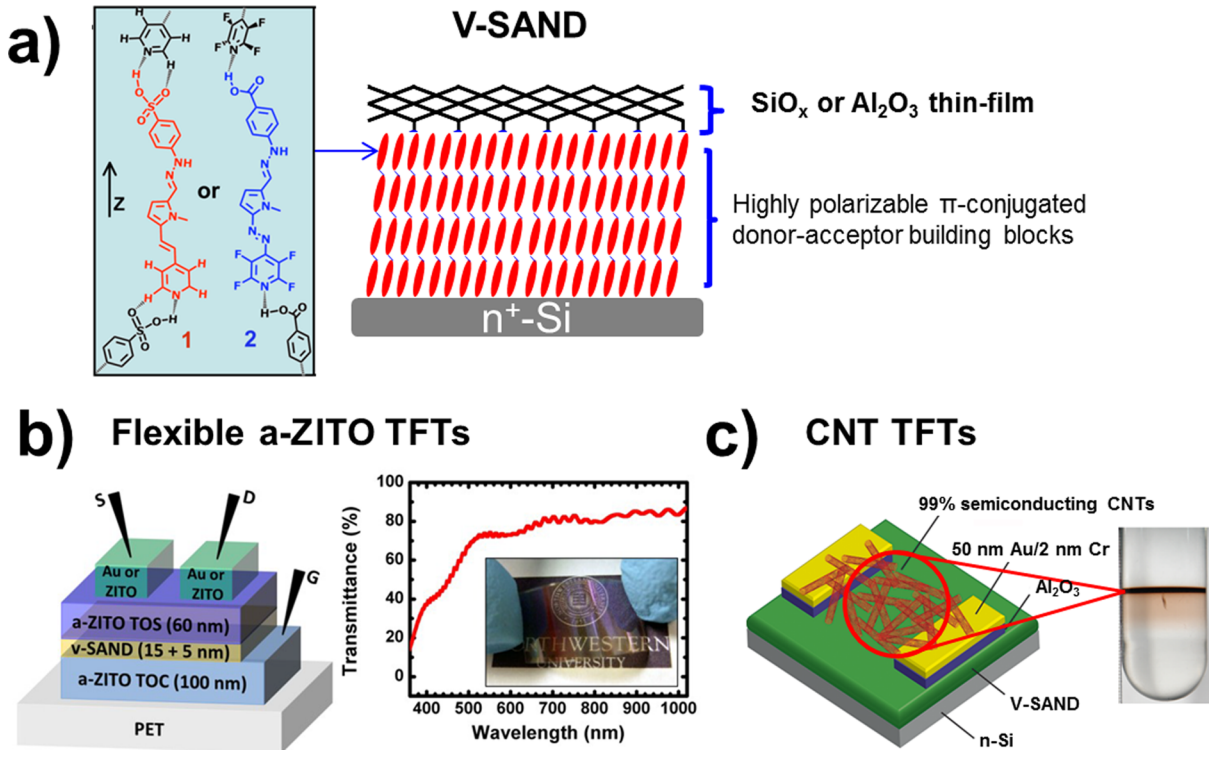

Figure 6. (a) Schematic representation of vapor-deposited self-assembled nanodielectrics (V-SAND) and chemical structures of organic components **1** and **2**. (b) Architecture and transmission optical spectrum (inset, a photograph of the TFT array bent over a printed Northwestern University seal) of transparent flexible a-ZITO thin-film transistor fabricated on a plastic substrate with the indicated materials. Adapted with permission from ref 42. Copyright 2011 Wiley-VCH Verlag GmbH & Co. KGaA. (c) Schematic of random SWCNT TFT fabricated on V-SAND using high purity (99%) semiconducting carbon nanotube film. Adapted with permission from ref 35. Copyright 2012 American Chemical Society.

interface traps, and remote polar phonons that are otherwise disruptive to semiconductor carrier transport.

3. HYBRID MULTILAYER DIELECTRICS BY VAPOR PHASE DEPOSITION

A complementary approach to accessing multilayer hybrid dielectrics with large gate capacitances is possible via solvent-free vapor-phase self-assembly, V-SAND (Figure 6). V-SANDs can be grown with precise thickness control and combine layers of highly polarizable π-conjugated donor–acceptor building blocks, self-assembled via hydrogen bonding, with ultra-thin layers of vapor-phase deposited SiO_x or ALD-derived Al_2O_3 to enhance stability and dielectric characteristics. Note that the dielectric response of the two types of molecular constituents,

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Table 1. Summary of Dielectric and TFT Characteristics for SANDs with Various Semiconductors

dielectric	capacitance (nF/cm^2)	I_G[a]	semiconductor[b]	μ (cm^2 V^{-1} s^{-1})	I_{ON}/I_{OFF}	V_T (V)	SS (V decade^{-1})	ref
Si-SAND	~180	10^{-8} A/cm^2	ZnO NW	~198	10^4	−0.4		16a
	~180	30−40 pA (4 V)	In_2O_3 NW	~1450	10^6	0.0		16b
	~180		SnO_2 NW	~172	10^6	−1.9		16c
	~170	~10 nA (1 V)	SWCNT	5.6	10^7	0.2		18
			In_2O_3 thin-film (IAD)	~120	10^5	0.1	0.09	19
			In_2O_3 thin-film (IAD) flexible	20	10^4			20
	~180	3.9 pA (1 V)	Si-Nanomembrane	~680	10^7	−1.1	0.12	21
	~270	1×10^{-7} A/cm^2 (4 V)	CdSe (CBD)	57	10^5	2.5	0.26	22
			In_2O_3 (SC)	44	10^6	2.2	0.3	23
			ITO (SC)	10−20	10^4			24
			ZITO (SC)	90	10^5		0.2	25
	~200	1×10^{-6} A/cm^2 (1 MV/cm)	ZITO (PLD)	~140	10^5	0.2	0.13	26
Zr-SAND	398	~3×10^{-7} A/cm^2	pentacene (PVD)	0.74	10^6	−0.6		29
	398	~3×10^{-7} A/cm^2	PDIF-CN_2 (PVD)	0.79	10^4	0.01		29
	465	~3×10^{-7} A/cm^2	ZTO (SC)	3.5	10^7	−1.1	0.12	29
	450		IYO (SC)	7.3 (300) 5.0 (250)	10^5			30
Hf-SAND	1100	~1×10^{-7} A/cm^2	SWCNT (99% semiconducting purity)	137	10^6	0.5	0.15	32
	630	<10^{-8} A (2 V)	IGZO (IJ)	20.6	10^7	~0	0.19	39
V-SAND	390	10^{-5}−10^{-7} A/cm^2 (2 V)	pentacene	2.4	10^5	1		40
	220	10^{-6}−10^{-7} A/cm^2 (1 MV/cm)	ZITO (PLD)	110	10^4	0.2	0.13	41
	630	10^{-7} A/cm^2 (1 V)	SWCNT (99% semiconducting purity)	147	10^5	−1.1	0.15	35

[a]Measured at 2 MV/cm, unless noted in parentheses. [b]IAD = ion-assisted deposition; CBD = chemical bath deposition; PLD = pulsed laser deposition; PVD, physical vapor deposition; SC = spin-coating. IJ = inkjet-printing.

1 and **2**, are enhanced by (i) their ability to self-assemble via head-to-tail hydrogen-bonding and (ii) molecular polarizabilities that are optimized[40] via computation-assisted design. It was demonstrated that the MIS and TFT device electrical properties are sensitive to the changes in microstructural organization such as introducing organic−inorganic alternating and nonalternating arrangements.[41] Pentacene TFTs fabricated with V-SAND exhibit large mobilities, ~3 cm^2 V^{-1} s^{-1}, and $I_{ON}/I_{OFF} \approx 10^5$ for optimized TFT performance. More importantly, this computation-assisted dielectric provides key molecular and thin-film structural information on how to design even higher performance gate dielectric films using self-assembled materials. V-SAND dielectrics are evidently promising for future flexible organic electronics requiring low-temperature, solvent-free deposition conditions.

The compatibility of V-SAND with amorphous TOS thin films was demonstrated by combining Zn−In−Sn−O (ZITO) thin films grown by pulsed-laser deposition (PLD) from a $Zn_{0.33}In_{1.40}Sn_{0.27}O_3$ target at 25 °C under O_2 partial pressure. Completely transparent TFTs with good mechanical flexibility were realized by integrating an a-ZITO channel, a TCO electrode, and V-SAND on flexible PET substrates to enable fully transparent TFTs[42] exhibiting 110 cm^2 V^{-1} s^{-1} mobility, 1.0 V operation, $I_{ON}/I_{OFF} \approx 10^4$, V_T = 0.2 V, and SS = 0.13 V decade^{-1}.

In a subsequent study, V-SAND gate dielectrics were integrated with high-purity semiconducting SWCNT films as the active layer to achieve TFT performance unconstrained by traditional trade-offs, such as trading large I_{DS} or μ for low I_{ON}/I_{OFF} or steep SS for low overall I_{DS}.[33] Thus, the resulting devices simultaneously exhibit <4 V operating voltages, SS = 0.15 V decade^{-1}, high normalized on-state conductance (8.5 μS/μm), high normalized transconductance (6.5 μS/μm), and high intrinsic field-effect mobility (147 cm^2 V^{-1} s^{-1}) with high $I_{ON}/I_{OFF} = 5 \times 10^5$ in ambient conditions. This landmark and record-setting process of combining hybrid gate dielectrics with semiconducting SWCNTs is compatible with low-temperature, large-area processing, thus offering great potential in low-power TFT-based electronics. These devices also exhibit negligible hysteresis in transfer characteristics, unlike those fabricated with conventional oxide dielectrics, and avoid the ambipolarity that increases power consumption for SWCNT TFT circuits based on ionic gel-based dielectrics.[43]

4. CONCLUSIONS

Novel molecule-scale organic−inorganic hybrid materials useful for overcoming the performance and processing limitations of conventional gate dielectric oxides (e.g. SiO_2) have been discussed in this Account. SANDs have proven compatibility with a wide range of unconventional semiconductors, often leading to enhanced transport properties (Table 1), with an advantageous component modularity affording ready adaptations to specific semiconductors and applications. This contribution also illustrates how reduced transistor operating bias voltage along with tunable optical transparency, processability, and environmental stability, makes SAND concepts of unique value to the future of high-performance unconventional electronics, including mechanically flexible, optically transparent, and high throughput roll-to-roll printed digital circuitry.

Future SAND-semiconductor integration, process/deposition refinement, and component synthesis (π-organic layer) strategies not only offer research opportunities but are needed to support continual advances in semiconductor and electronics applications. For example, efforts aimed at tuning surface density and packing motif of the π-electron constituents by selection of

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specific metal oxide layers is a promising avenue just beginning to be explored and may dramatically affect layer dielectric constant and overall dielectric performance. Furthermore, the synthesis of new π-electron constituents may offer additional benefits in enhancing dipolar polarizability, surface organization, or assembly rates. Thus, the intensive research efforts devoted to date in new semiconductors motivate complementary efforts in gate dielectric materials that offer compatible manufacture with the semiconductor, including solution or vapor phase processing, affording SAND-like materials relevant for electronic technologies.

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